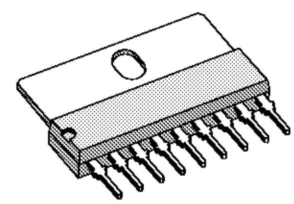
SGS-THOMSON MICROELECTRONICS

TDA8143

HORIZONTAL DEFLECTION POWER DRIVER

- CONTROLLED DRIVING OF THE POWER TRANSISTOR DURING TURN ON AND OFF PHASE FOR MINIMUM POWER DISSIPATION AND HIGH RELIABILITY
- HIGH SOURCE AND SINK CURRENT CAPABILITY
- DISCHARGE CURRENT DERIVED FROM PEAK CHARGE CURRENT
- CONTROLLED DISCHARGE TIMING
- DISABLE FUNCTION FOR SUPPLY UNDER VOLTAGE AND NONSYNCHRONOUS OPERATION
- PROTECTION FUNCTION WITH HYSTERESIS FOR OVERTEMPERATURE
- OUTPUT DIODE CLAMPING
- LIMITING OF THE COLLECTOR PEAK CURRENT OF THE DEFLECTION POWER TRANSISTOR DURING TURN ON PERIOD
- SPECIAL REMOTE FUNCTION WITH DELAY TIME TO SWITCH THE OUTPUT ON



SIP9
(Plastic Package)

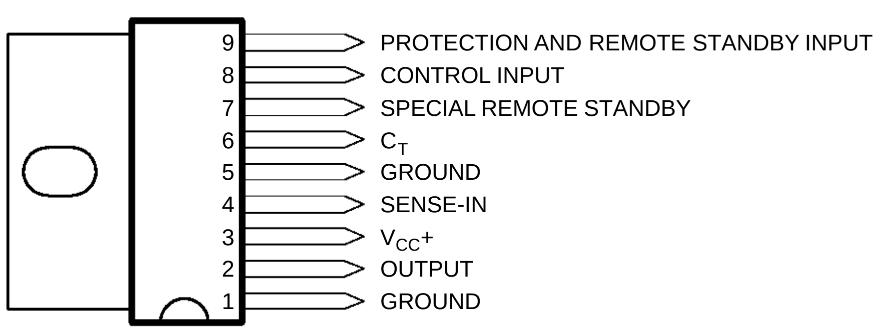
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DESCRIPTION

The TDA8143 is a monolithic integrated circuit designed to drive the horizontal deflection power tran-sistor.

The current source characteristic of this device is adapted to the non-linear current gain behaviour of the power transistor providing a minimum power dissipation. The TDA8143 is internally protected against short circuits and thermal overload.

PIN CONNECTIONS



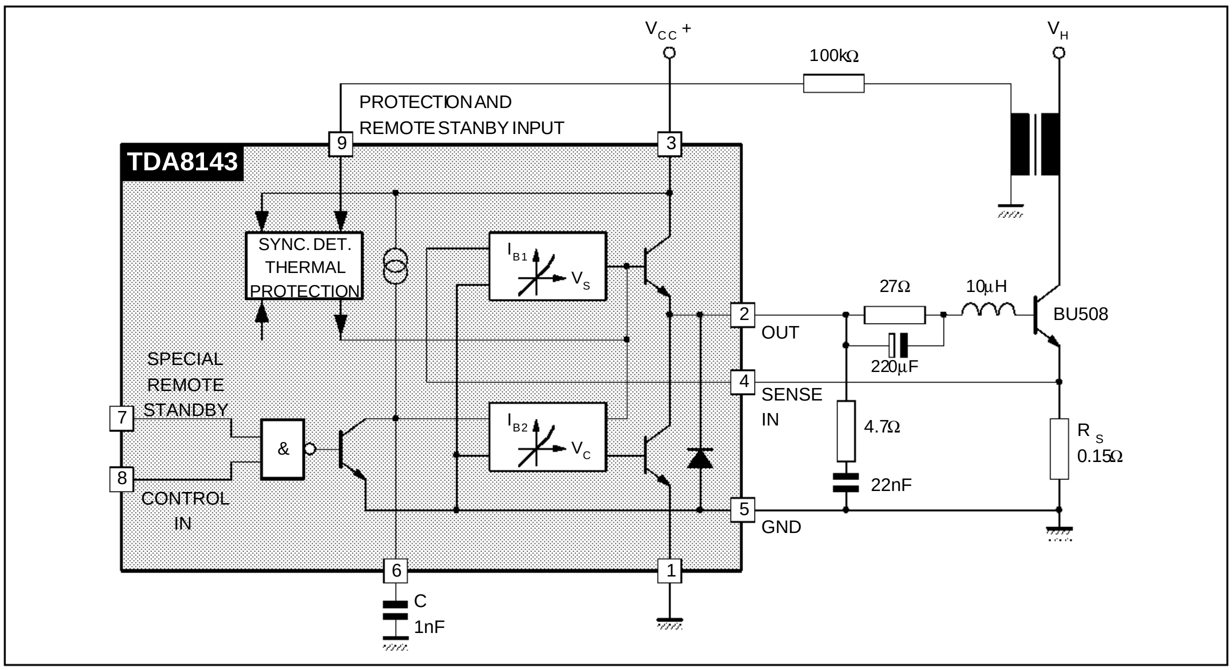
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PIN FUNCTIONS

Pin	Name	Function
1	Power Ground	Common Ground
2	Ouptut	Device Output
3	V_{CC}	Supply Voltage
4	Sense Input	Input voltage that determines output current.
5	Sense GND	Reference Ground for Input Voltage at SENSE INPUT.
6	C_{EXT}	Capacitor between this terminal and SENSE GROUND determines the current slope dI_O/dt during OFF phase.
7	Special Remote/Standby	Low level at this input sets the device after a delay time t_{dr} in the standby mode independent from CONTROL INPUT (2nd priority).
8	Control Input	High level at this input switches the BU508 off, low level switches the BU508 on.
9	Protection and Remote Standby Input	A high level at this input switches the BU508 off independent from all other inputs (1st priority).

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BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	18	V
I_d	Output Current	Internally Limited	
P_{tot}	Power Dissipation	Internally Limited	
T_{stg}, T_j	Storage and Junction Temperature	– 40, + 150	°C
T_{oper}	Operating Temperature	0, + 70	°C

8143-02.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j–a)}$	Thermal Resistance Junction-ambient	Max.	70	°C/W
$R_{th\ (j–c)}$	Thermal Resistance Junction–case	Max.	10	°C/W

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ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		7		18	V
I_Q	Quiescent Current	All Inputs Open	10	15	25	mA
I_{p0}	Positive Output Current (source)		1.5			A
I_{n0}	Negative Output Current (sink)		2			A
I_{o0}	Positive quiescent output current forcing the output to 6 V and the sense input to ground output externally forced to 6 V.	Remote Input1 Remote Input0	120 50	150 80	200 100	mA mA
G_{ON}	Transconductance ON Phase (1)	See Figure 1	1.8	2.0	2.2	A/V
G_{OFF}	Transconductance OFF Phase (2)	See Figure 1	1.8	2.0	2.2	A/V
G_{REMOTE}	Transconductance Standby Mode	Remote Input0	0.675	0.75	0.825	A/V
I_5	Current Source Pin 6	V_7 = 500 mV	135	165	200	µA
R_{INS}	Sense Input Resistance	$V_S > 0$ $V_S < 0$	0.7 0.35	1 0.5	1.3 0.7	kΩ kΩ
I_{INS}	Sense Input Bias Current	$V_S = 0$ Remote Input = 1	– 200	– 300	– 400	µA
R_{SYN}	Synchronous Detection Input Resistance	$V_{SYN} < 7$ V $V_{SYN} > 7$ V	30 7	60 10	150 15	kΩ kΩ
V_{THS}	Threshold Voltage of the Synchronous Detection Input		1	1.8	2.8	V
V_{SYN}	SYNC DETECT Input Voltage				30	V
V_{THA}	Threshold Voltage of Control Input		1.5	2	2.5	V
I_{INA}	Pull up Current of Control Input	$0 < V_{IN} < V_{THA}$ $V_{IN} > V_{THA} + 0.5$ V	– 50 – 1	– 100 0	– 160 + 1	µA µA
V_{THB}	Threshold Voltage Remote Input		1.5	2	2.5	V
I_{INB}	Pull-up Current of the Remote Input	$0 < V_{IN} < V_{THB}$ $V_{IN} > V_{THB} + 0.5$ V	– 50 – 1	– 100 0	– 160 + 1	µA µA
t_{dr}	Remote Delay Time (3)		190	250	300	µs
t_{don}	On Delay Time			3	4.5	µs
$V_{CC}–V_{OUT}$	Output Voltage Drop for I_{p0} = 1 A		2	2.8	3	V
$V_{CC\ ON}$	Supply Voltage for Device "ON"	$I_0 \geq 0$	5.8	6.4	7.0	V
$V_{CC\ OFF}$	Supply Voltage for Device "OFF" (output internally switched to ground)		5.6	$V_{CC\ ON}$ – 0.2 V	6.8	V
$V_{S\ limit}$	Sense Limit Voltage (4)		0.8	0.9	1	V

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Notes :
1. G_{ON} is measured with V_4 varying from 150mV to 350mV (Pin 6 is grounded)
2. G_{OFF} is measured with V_6 varying from 150mV to 350mV (Pin 4 is grounded)
3. When the remote input goes from HIGH to LOW the BU508 is switched off and it remains in this condition for the time t_{dr}.
4. The sense input voltage V_S is internally limited and results in a limited positive output current I_{p0} = g. V_S limit. Note that due to the storage time t_S of the BU508 limiting of V_S leads to a reduced base current of the BU508 and the output current I_0 is going to the positive quiescent current I_{o0}.

TRUTH TABLE

Logics Inputs		Output I_0		Mode
Control Input	Remote/Standby			
0 Floating or 1	Floating or 1 Floating or 1	$I_0 > 0$ $I_0 < 0$ (5)	BU508 ON BU508 OFF	Normal Function
X	0	$I_0 < 0$ (5) $0 < t < t_{dr}$	BU508 OFF	Remote/Standby Function
X	0	$I_0 > 0$ $t > t_{dr}$	BU508 ON	

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Note : 5. $I_O < 0$ means that the sink current flows into the output to ground.

Figure 1 : $\frac{G_{ON}}{V_{Pin3}}$ and $\frac{|G_{OFF}|}{V_{Pin5}}$

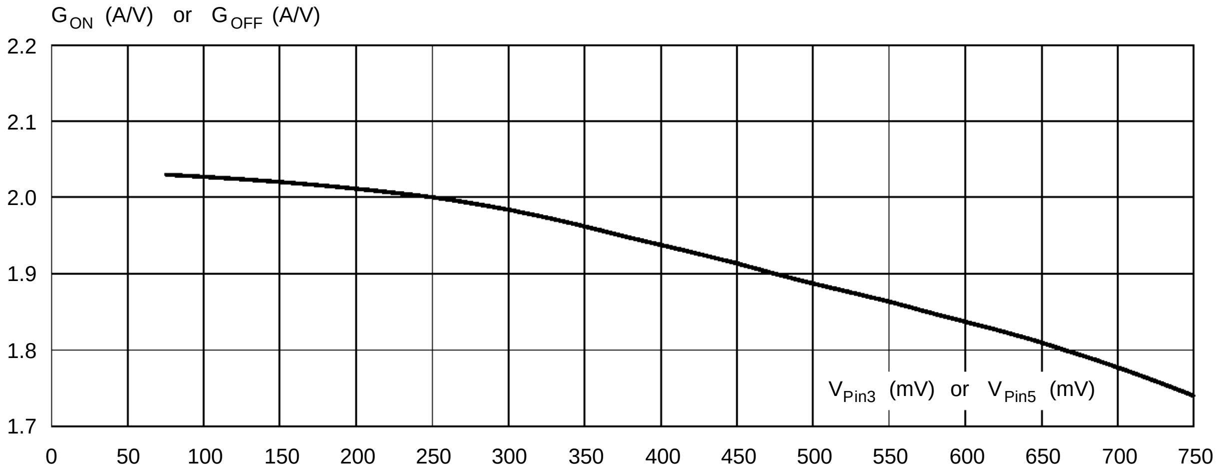
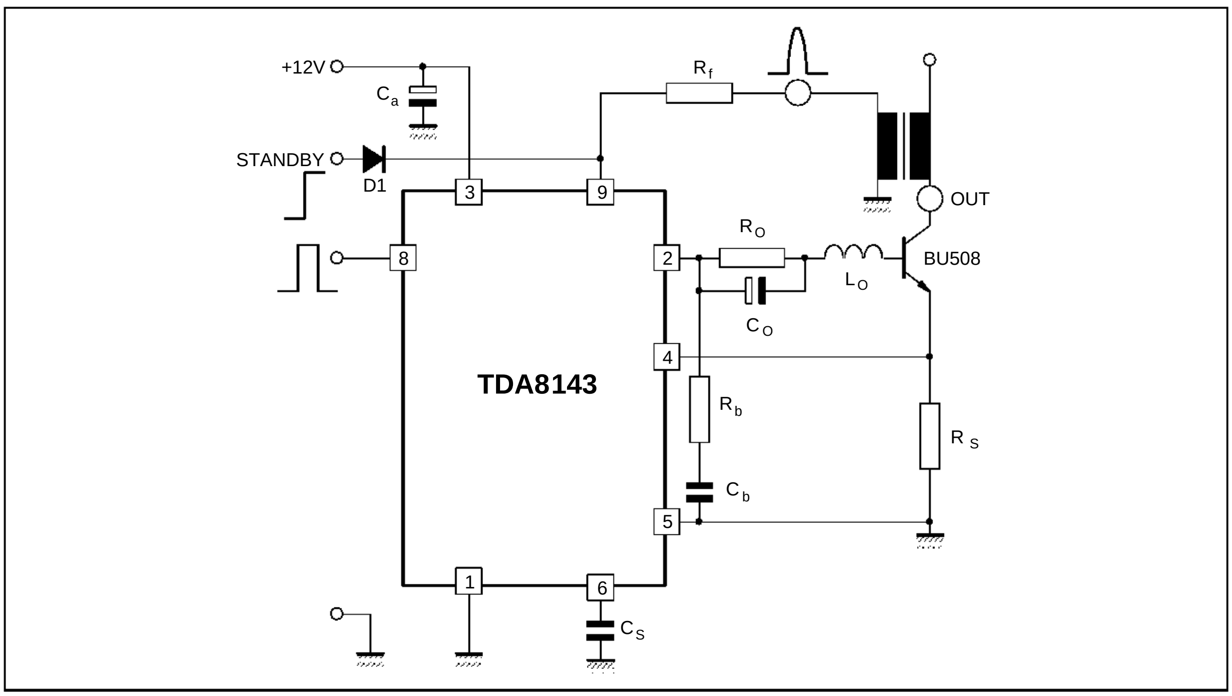


Figure 2 : Large Screen Application



COMPONENTS LIST FOR TYPICAL APPLICATION

CRT	22"/26" 100°	14"/20" 90°	CRT	22"/26" 100°	14"/20" 90°
C_a	47 μF	47 μF	R_b	4.7 Ω	4.7 Ω
R_o	27 Ω 2W	27 Ω 1 W	C_b	47 nF	47 nF
C_o	220 μF	220 μF	R_s	0.15 Ω	0.1 Ω
L_o	10 μH	10 μH	C_s	1 nF	1 nF

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APPLICATION INFORMATION

The conventional deflection system is shown in Figure 3. The driving circuit consists of a bipolar power transistor driven by a transformer and a medium power element plus some passive components.

During the active deflection phase the collector current of the power transistor is linearly rising and the driving circuitry must be adapted to the required base current in order to ensure the power transistor saturation.

According to the limited components number the typical approach of the present TVs provides only a rough approximation of this objective ; in Figure 4 we give a comparison between the typical real base current and the ideal base current waveform and the collector waveform.

The marked area represents a useless base current which gives an additional power dissipation on the power transistor.

Furthermore during the turn-ON and turn-OFF transient phase of the chassis the power transistor is extremely stressed when the convenctional network cannot guarantee the saturation ; for this reason, generally, the driving circuit must be carefully designed and is different for each deflection system.

The new approach, using the TDA8143, overcomes these restrictions by means of a feedback principle.

As shown in Figure 4, at each instant of time the ideal base current of the power transistor results from its collector current divided by such current gain which ensure the saturation ; thus the required base current I_b can be easily generated by a feedback transconductance amplifier g_m which senses the deflection current across the resistor R_s at the emitter of the power transistor and delivers :

$$I_b = R_S \bullet g_m \bullet I_e$$

The transconductance must only fulfill the condition :

$$\frac{1}{1+\beta min} \cdot \frac{1}{R_S} < gm < \frac{1}{R_S}$$

where β is the minimum current gain of the transitor. This method always ensures the correct base current and acts time independent on principle.

For the turn-OFF, the base of the power transistor must be discharged by a quasi linear time decreasing current as given in Figure 5.

Conventional driver systems inherently result into a stable condition with a constant peak current magnitude.

Figure 3 : Conventional Horizontal Deflection System for TVs

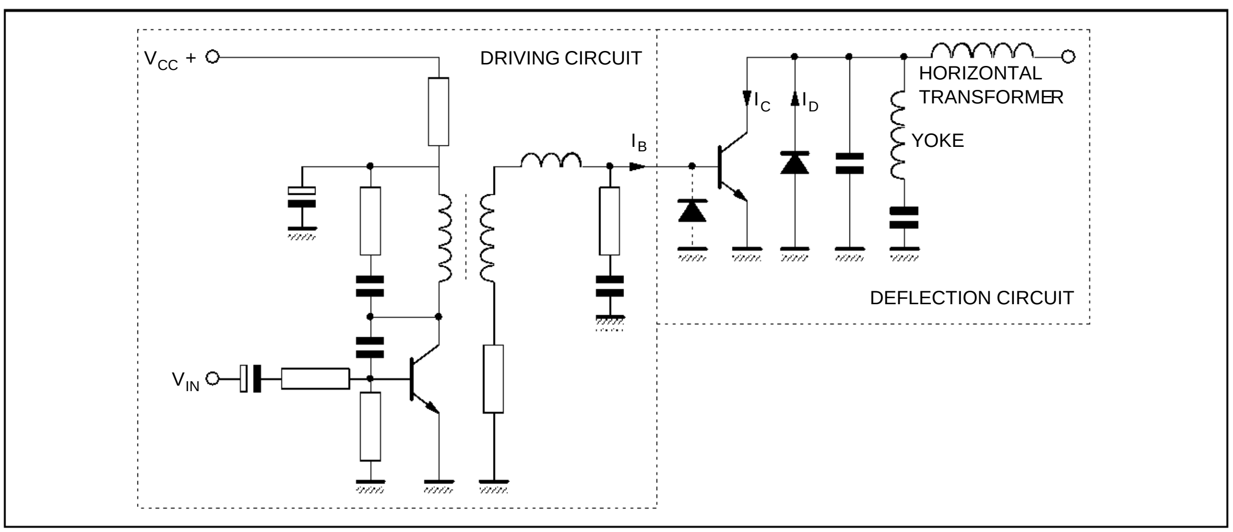
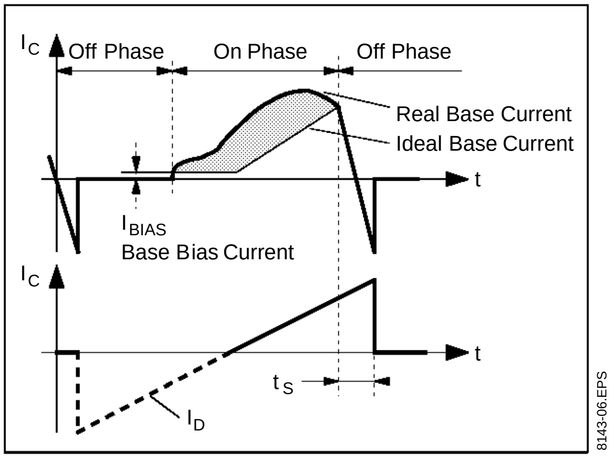


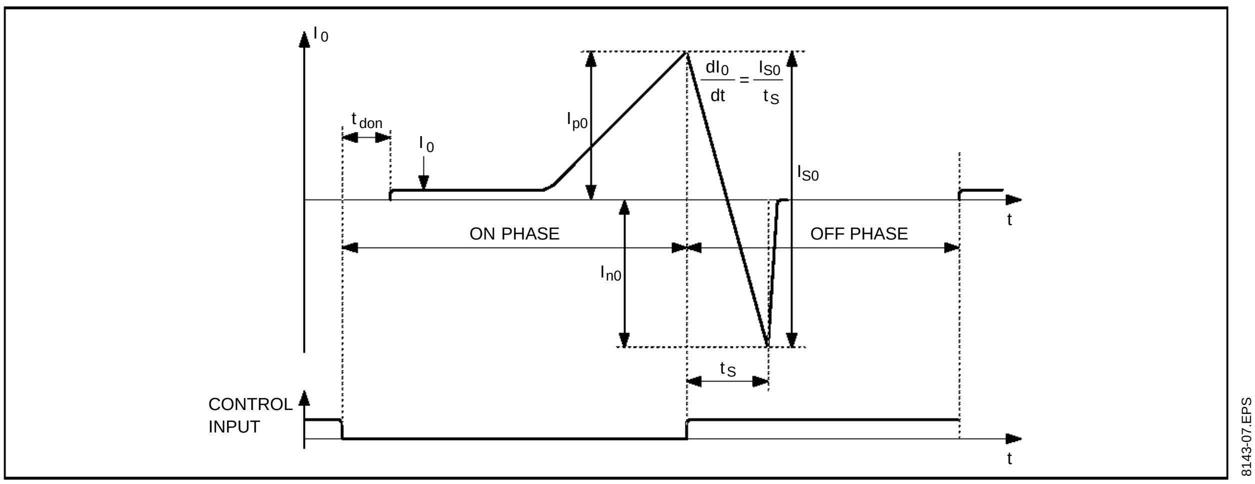
Figure 4 : Waveforms of Collector and Base Current



This is due to the constant base charge in the turn-ON phase independent from the collector current ; hence a high peak current results into a low storage time of the transistor because the excess base charge is a minimum and vice versa. In the active deflection the required function, high peak current-fast switch-OFF and low peak current-slow switch-OFF, is obtained by a controlled base discharge current for the power transistor ; the negative slope of this ramp is proportional to the actual sensed current.

As a result, the active driving system even improves the sharpness of vertical lines on the screen compared with the traditional solution due to the increased stability factor of the loop represented as the variation of the storage time versus the collector peak current.

Figure 5



CIRCUIT DESCRIPTION

Figure 6 shows the block diagram of the TDA8143, the circuit consists of an input transconductance amplifier composed by Q1, Q2, Q3 and Q4.

The symmetrical output current is fed into the load resistor R1 and R2 ; the two amplifiers V1 and V2 realize a floating voltage to current converter which can drive 1.2A sink current and 2A source current for a wide common output range.

So, the overall transconductance results into :

$$g_m = \frac{R1 + R2}{R3} \cdot \frac{1}{R5}$$

A current source I_1 generates a drop of 70mV across the resistor R4 which provides an output bias current of 140mA; the control input determines the turn ON/OFF function.

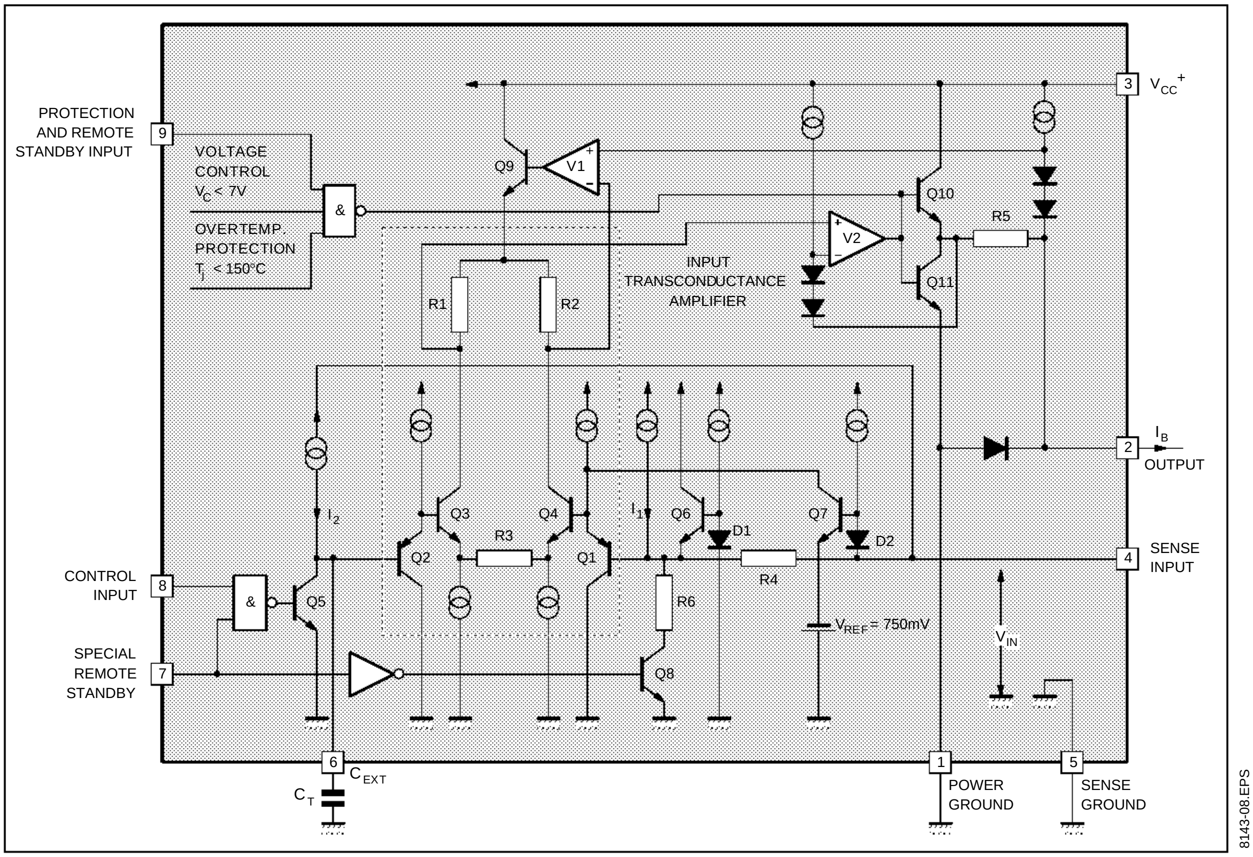
In the ON phase, Q5 shorts the external capacitor C_t. Within the input voltage range $0 < V_{in} < 750mV$ the element realizes the transconductance function ; lower voltages are clamped by the D1/Q6 configuration.

For input voltages higher than 750mV, Q7 limits the maximum output current at 1.5A peak.

In the turn-OFF mode, C_t will be charged by the controlled source I_2 which is proportional to the input voltage, by this way, the output current decreases quasi linearly and the system stability is reached.

During the flyback phase, the IC is enabled via the sync. detector input ; this function with the limited sink and source current together with the undervoltage turn-OFF and a chip temperature sensor ensure a complete protection of the IC.

Figure 6 : Block Diagram of the Integrated Horizontal Driver



In Figure 7 is shown the application diagram of the TDA8143, the few external component and the automatic handling possibility ensures a lower application cost versus the conventional approach shown in Figure 3.

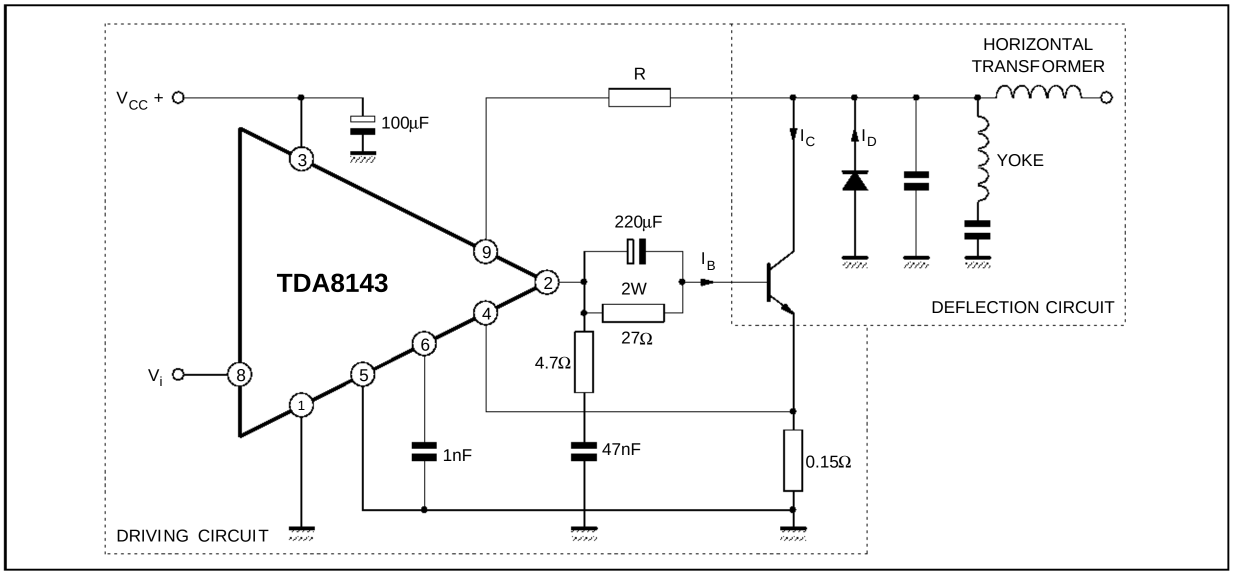
In Figure 8 is shown the currents and voltage waveforms of the driver circuit of Figure 7 as to be seen, the driving charge $I_b \cdot t_{on}$ has been reduced at minimum.

The power dissipation on this application condition is about 1.3W.

The presence of thermal shut-down circuit means that the heatsink can have a smaller factor of safety compared with that of a conventional circuit.

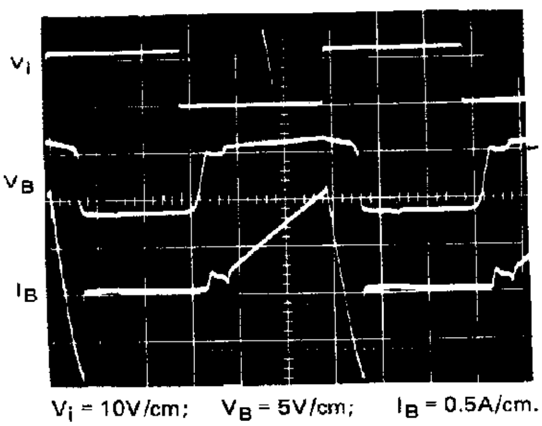
If for any reason, the junction temperature increases up to 150^{o}C, the thermal shut-down simply switches off the device.

Figure 7 : Integrated Horizontal Driver

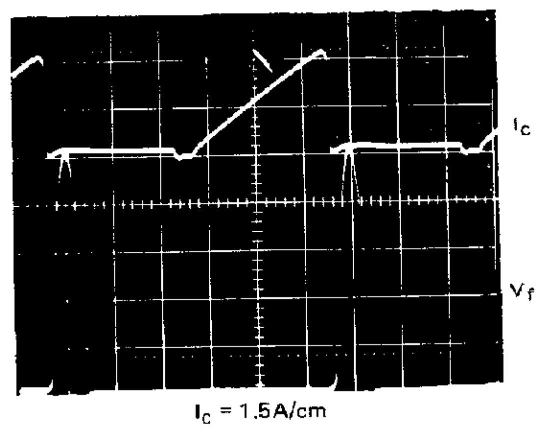


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Figure 8 : Signal Diagrams of the Driver Circuits



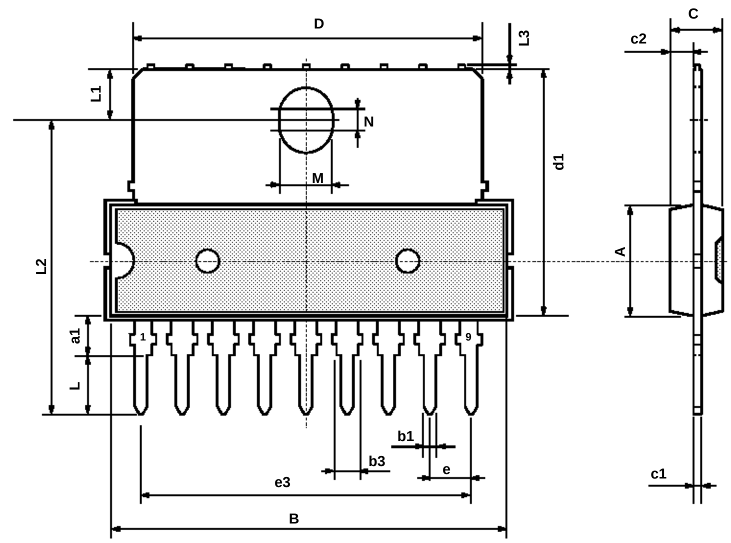
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PACKAGE MECHANICAL DATA

9 PINS - PLASTIC SIP



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Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

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